

# ROHIT KUMAR

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## EDUCATION

- **Master of Science, ECE-Computer Engineering** *Aug 2008 - May 2010*  
**GPA - 3.56/4.0**  
University of Florida, Gainesville, FL USA
- **Bachelor of Engineering, Electronics and Communication** *Aug 2002 - May 2006*  
**GPA - 7.13/10**  
Institute of Technology,  
Banaras Hindu University, India

## COURSES

- Computer Architecture
- Parallel Computer Architecture
- Fault-tolerant Computer Architecture
- Distributed Computing(enrolled)
- Reconfigurable Computing
- Digital Signal Processing
- Digital Filtering
- Embedded Systems(enrolled)

## SKILLS SUMMARY

### **2 Yrs of Industry Experience in hardware/software co-design.**

Proficiency in tools from Xilinx (ISE, ChipScope, PlanAhead), Mentor Graphics (Modelsim), familiarity with Nallatech(Dimetalk) and Aldec Riviera-Pro

**Languages:** VHDL, C, MATLAB, MPI (MPICH 1.1), UPC, Assembly, Embedded C, C++

**OS and Software:** Ubuntu Linux, Solaris 7, Windows, MS-Office Suite, LaTeX

**Hardware:** Xilinx FPGA Boards (ML505, ML401), PIC Microcontrollers, RS-232 and USB interface

**Analysis Methods:** Petri-Nets (generic, timed and stochastic), Markov chain modeling

## ACADEMIC PROJECTS AND PUBLICATIONS

### **MACS: A Minimal Adaptive Routing Circuit-Switched Architecture for Scalable and Parametric NoCs**

R. Kumar and A. Gordon-Ross. IEEE International Conference on Field-Programmable Logic and Applications (FPL), August 2009  
( VHDL, Xilinx ISE 11.2i, PlanAhead 11.2, ISim, Modelsim 6.4, ChipScope 11.2 )

**Design and development of MIPS based assembler and simulator** *( C/C++ ) - 4 members*

**FPGA based Fibonacci Compressor/De-compressor and encoder/decoder** *( VHDL, DIMETALK ) - 4 members*

**jsMPI: javaScript bindings for MPI** *( MPICC, Google V8 javaScript engine ) - 3 members*

**Design and Implementation of a Bus Communication Architecture for Run-Time Partial Reconfigurable FPGA based SoC** *( VHDL, Xilinx ISE 7.1i ) - 2 Members*

**GSM Filter Design ( IIR & FIR ), Implementation, Testing and Performance Analysis** *( MATLAB )*

**Conditional Rejuvenation in HPC Systems based on Failure Prediction via Machine Learning** *( MATLAB )*

## WORK EXPERIENCE AND PROFESSIONAL ACTIVITIES

### **Research Assistant, NSF Center for High performance Reconfigurable Computing (CHREC) Jan 2009 - present**

- Design and analysis of high performance communication architecture ( NoC ) for FPGA based SoC
- Case study of target tracking application, employing in-house Kalman filter core, on FPGA based NoC
- Partially reconfigurable architectural exploration of applications by analysis of formal specification

### **Reviewer (Secondary)**

- IEEE International Symposium on High-Performance Computer Architecture, Jan 2010
- International IEEE Symposium on Field-Programmable Custom Computing Machines, May 2010

### **Design Engineer, ST Microelectronics, India**

*March 2007 -Aug 2008*

- 12-segement display controller DMA channel in STi71xx, STi55xx high definition set-top box decoder chip, this work saved 0.01EUROS per chip
- NAND SEC/DED flash controller DMA channel in STi71xx, STi72xx high definition set-top box decoder chip

### **Software Engineer, MOTOROLA, India**

*June 2006 - Feb 2007*

- Development and enhancement of DCT's and ASTB's (Motorola Set-top Boxes) firmware layer. Implemented the infrastructure for home networking of Set-top box with remote WH-DVR feature